Gary Feierbach – CV

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Summary:
Looking to contribute with emphasis on robotics, big data, parallel languages, algorithm design, embedded systems, and have an engineering management and hands-on role in the designing, building and testing prototype systems.

Publications, Patents, and some References on LinkedIn, Research Gate
Additional References on Request.

Employment Highlights:
2010 - 2016
Owner Inner Access Consulting

- Currently creating Julia language videos for PackT. Also writing AI routines in Julia
- Lunchtime keynote speaker at 2015 “Robotics as a business” mini-conference in San Mateo California.
- Consulting (software – embedded, system and application, hardware - digital and some analog, commercial website back-end and front-end development)
- Engineering Management, Engineering Research and Technical Writing)
- Operating Systems: Windows, OSX, Linux, Unix
- Software used: Julia, C, C++, ObjectiveC, Java, JSPs, Javascript, Perl, Python, PHP, AJAX, database MySQL, Verilog, graphics OpenGL, Spark, Unix/Linux shell scripts, Assembly Language on many machines
- Office Suites (MS and OpenOffice), PC Layout Software, Adobe Photoshop, Various development systems like MPLabX
- More than a dozen patents over several technologies.

2005 – 2009
CEO Tamago
Tamago was a web store and a peer-to-peer e-commerce system for the distribution of digital media.

- Raised Angel funds to complete design phase.
- Dealt with marketing, sales, digital media suppliers and our web presence.
- Designed and implemented the search advertising subsystem (java, JSPs).

2004 - 2005
CEO/CTO Inner Access LLC
Provide technical support and advice to high tech startups.

1999 – 2003 Apple Computer
VLSI Verification Manager
This consists of a team of 20 engineers dedicated to making sure that the design of the many complex north and south bridge chips, designed at Apple, would work on their first try. All chips designed during my tenure achieved this and only a few minor metal changes were necessary for full functionality.

While recruiting, motivating and managing a group of very talented engineers I also applied for several patents, wrote code to simulate various pieces of hardware such as synchronizers and fifos, wrote the VLIW assembler, disassembler and code checker for a built-in north bridge codec, developed a variety of Perl scripts and developed new technologies for verification (true coverage).

1998-1999 Racer Graphics
(bought by Apple in late 1999)
Manager of Computer Modeling

- With a team of 5 programmers build an extremely complex C++ model of the Racer OpenGL Graphics engine (~800 pipelined stages). The model was used both for architectural studies and as a co-simulation tool with the Graphic Engine RTL for random and directed tests. I also managed design verification CAD, Directed and Random test development, test bench development and the regression testing effort.

1994 -1998 Sun Microsystems – Sun Microelectronics division

- Media Java Project -- Verification Manager and Architectural contributor
  This project combined the Java Engine II core with a memory controller, graphics controller, MPEG II decoder and a PCI interface.
- Eagle Project – Verification Manager
  This project combined the microSparc II core with a memory controller and a PCI interface. Project completed on time, First silicon booted OS.
- Magellan Project – Logic Manager
  Combined the core of the UltraSparc II with a memory controller and PCI interface and eliminated the secondary cache.
- Spitfire Project – Sr. Emulation team member
  Emulated the UltraSparc I processor on the QuickTurn Enterprise System. This involves writing a number of C and Perl programs and scripts to make the data conform to QuickTurn hardware and software requirements.
- Taught an embedded systems programming class at U.C. Santa Cruz Extension.
- Applied for and received several patents and coauthored a paper on emulation.

1988-1994 Intergraph Corporation, Advanced Processor Division, Palo Alto, CA
(This division was sold to Sun Microsystems)
Staff Engineer to the Director of Engineering

- Converted logic design of advanced floating-point unit from ADX to Verilog and completing the design for the next generation processor.
- Used HSpice and Greenfield tools in conjunction with some C code and UNIX scripts to do a detailed transmission line analysis of long on-chip paths. Used these same tools to create the process dependent parameters for a Dracula LPE extraction for on-chip wire capacitance and resistance for back annotation in Motive timing analysis.
- Enhanced existing C4 diagnostic monitor by adding disassembly, break-point and program patching capability.
- Wrote a number of diagnostics to track down problems in the C4M asynchronous memory controller unit and MCM module.
- Did logic design of a myriad of memory boards for the QuickTurn emulation system to emulate C4I cache and memory management and C4M memory controller chips. These included I&D cache, I&D tag ram, triple four port 64-bit register file and 1Gb main memory dynamic ram boards.
- Wrote a number of C programs and scripts to automate various board and chip design activities. These made extensive use of UNIX utilities and Intergraph's graphics database.
- Brought up VME to QuickBus Interface; wrote test software in C and assembler to wring out design, modified VME disk driver for off the shelf controller to bring up UNIX (needed to make FFS modifications.)
- Designed several test fixtures and production chip set modules.

Manager - Systems Engineering

- Responsible for tracking down causes of chip failures from circuit and logic design through layout and fabrication. This involved coordinating the activities of several departments and my own crew of diagnostic programmers, device physicists, engineers and technicians. Was able to cut diagnosis time from weeks to days, even for very difficult problems.
- Also wrote neural net software exploiting Mark Jurik's back percolation algorithm (in C) to explore its use for yield prediction from parametric data.

Manager, Chip Floor Planning

- Responsible for floor planning of high performance CMOS C421 floating-point processor; Involved in all aspects of committing a design to silicon.

(Also taught robotics courses at U.C. Santa Cruz extension during this period. The course placed a heavy emphasis on algorithms I had implemented in Forth and C.)

1979-1988 Inner Access Corporation, Foster City, CA
President and General Manager

- Responsible for administration and day-to-day operation.
- Supervised the design team of NOEL multi-user Motorola 68K series of computer systems.
- Designed and built specialized test equipment for the component boards of the above systems which included an automated program generator and forms generator.
- Designed a large database system for a telephone solicitation service.
- Participated in the design and implementation of a large public utility funded appliance energy conservation project
- Implemented Forth compiler/interpreters on a number of microprocessors.
- Personally taught both beginning and advanced Forth Classes.
- Designed and implemented software for mass spectrometer NBS library search on an IBM XT (ended up embarrassingly faster than DG NOVA software on a more sophisticated product of client.)
- Wrote disk drivers and a number of utilities for NOEL series.
- Designed and implemented a variety of Zilog Super8 based hardware and software products.
- Wrote most of the manuals for IAC boards and computers

1976-1979 Institute for Advanced Computation, Sunnyvale, CA
(The Institute for Advanced Computation was jointly sponsored by NASA and ARPA)
Computer Architect – Advanced Studies Department

- Co-architect of the Phoenix computer which was to eventually replace the ILLIAC IV. This state-of-the-art parallel 1040 processing element machine used a novel interconnection network approach which was self-repairing. Wrote a number of programs to simulate various components of the system.

Director of the Institute's Simulation Lab

- Responsible for simulation modeling activities on the ILLIAC IV. This included plasma particle codes, urban construction simulation and SETI activities.

Manager of ILLIAC IV enhancement group

- Responsible for bringing the ILLIAC IV to operational status.
  Supervised 30 engineers and technicians. This position was occupied by several talented people before me with no success. The institute was losing in excess of $2,000/hr in lost ILLIAC IV revenue which made this position a major focus of attention. My actions were systematic, thorough, and drastic, and achieved almost immediate success.

1974-1976 Minicomputer Technology, San Jose, CA
(Bought by EH International)
President and General Manager

- As founder, was involved in the design of high performance disk controllers for minicomputers. Controllers used track buffers, seek reordering and overlapping and PLL data detection. The controllers were for several minicomputer architectures and accommodated four Trident SMD drives.

1968.1974 Autologic Inc., Newberry Park, CA
(bought by Volt Information Sciences in 1973)
Vice President – Systems Development

- Manager of the Northern California Lab leading the design team which developed a sophisticated, highly successful, automated design system running on a Raytheon 704 computer.
- Devised the first program to use the A* AI search algorithm for the routing of printed circuit boards. Our router was smaller, faster, more flexible and had higher completion rates than our competition running on large mainframes.
- Devised the highly successful bounded channel algorithm for component placement.

1967.1968 Information Management Inc., San Francisco, CA
(Company and Name bought by Palo Alto firm now called Information Management International, Inc.)
Senior systems analyst.

- Implemented a computer model of a ballistic missile defense system for fleet protection.
- Implemented a computer model of the City of San Francisco residential housing sector in conjunction with ADL Inc.
- Implemented a COBOL syntax checker and preprocessor.
- Developed micrologic simulation incremental compiler
- Performed systems analysis and programming services for several departments at U.C. Berkeley, State Dept. of Public Health, State Water Quality Board, U.S. Dept. of Forestry and several local engineering and market analysis firms.

Education:
BA in Physics and Mathematics, 1963, U.C. Berkeley
MS Electrical Engineering and Computer Science, 1967, U.C. Berkeley

Programming languages, Assembler and O/S Experience:
Languages: Many variants of C, C++, C#, Perl, Tcl/Tk, Ruby, Java, JSP, Julia, Forth, Fortran, Cobol, Sybol, Snobol, Ajax, Javascript, HTML, CSS (and several others)
OS: Unix, Linux, Window 95, 98, 2000, XP, Mac OSX, MS/DOS, AMOS, D/OS
Assemblers: Intel 80xxx, 8048, 8051, Zilog Z80, Z8, Super8, Motorola 680xx, Power PC, Altivec, MicroChip PIC, (and others)
Other tools: OpenGL, Flash8, MySQL, Vera, Verilog, (and many others)

Hobbies: Writing Science Fiction (pen name Kalifer Deil), Painting, kinetic art, teaching robotics and computing using Raspberry Pi.